What is Claimed is:

1. A method for forming metal line of semiconductor device, comprising the steps of:

(a) sequentially forming a conductive layer for lower metal line and a conductive layer for via contact plug on a planarized first interlayer insulating film having a contact plug;

(b) etching the conductive layer for via contact plug and the conductive layer for lower metal line using a lower metal line mask to form a lower metal line;

(c) forming a second interlayer insulating film on the entire surface;

(d) etching the second interlayer insulating film and the conductive layer for via contact plug using a via contact mask to form a via contact plug;

(e) forming a third interlayer insulating film on the entire surface;

(f) performing a planarization process to expose a upper surface of the via contact plug; and

(g) forming an upper metal line electrically connected to the via contact plug.

2. The method according to claim 1, wherein the

conductive layer for lower metal line, the conductive layer for via contact plug and the upper metal line are respectively selected from the group consisting of aluminum layer, copper layer, tungsten layer, cobalt layer, silicon layer, and combinations thereof.

3. The method according to claim 1, wherein the via contact mask exposes a portion of the second interlayer insulating film above the lower metal line except a predetermined region where the via contact plug is to be formed.

4. The method according to claim 1, wherein the step (d) utilizes difference in etch selectivity between the conductive layer for lower metal line and the conductive layer for via contact plug.

5. The method according to claim 1, wherein the planarization process is an etch-back process or a CMP process.